IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Accompanying Continuation Application under 37 CFR 1.53:

Prior Application:	T. ISHII et al Serial No. 09/332,445 Filed: June 14, 1999
Group Art Unit:	2823
Examiner:	N. Berezny
For:	SEMICONDUCTOR ELEMENT AND PROCESS FOR MANUFACTURING THE SAME

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above application as follows.

IN THE SPECIFICATION

Please amend the specification as set forth below.

Page 13, the second full paragraph, lines 4 to 8, replace the paragraph with:

Fig. 25 illustrates a the prototype element having memory cells of 120 bits by repeatedly using the structure of the semiconductor element of Embodiment 6 of the present invention.

Pages 35 and 36, the paragraph bridging these pages from page 35, line 24 to page 36, line 12, replace the bridging paragraph with:

In Fig. 24, there is shown a structure in which four present structures are repeatedly arranged to have sixteen thin film regions. In Fig. 25, moreover, there is presented an [electron-microscope photograph] illustration of a prototype element which is prepared by arranging the present structures repeatedly and by arranging memory cells of 120 bits in a matrix. In the photograph, ten control electrodes run transversely. Six sets of three low-resistance regions run longitudinally (which correspond to the low-resistance regions 1 to 3 such that two of them correspond to the thin film regions 1 and 2 for one control electrode). There are arranged 10 x 6 x 2 = 120 thin film regions. In this large-scale memory, the writing, erasing and reading methods can be accomplished basically in an identical manner.

IN THE ABSTRACT

Please cancel the Abstract and substitute therefor the Abstract of the Disclosure on the attached separate page.

IN THE CLAIMS

Please cancel claim 1 without prejudice or disclaimer and add new claims 37-41 as set forth below.

--37. A semiconductor memory apparatus comprising:

a semiconductor memory device comprising a source region and a drain region, a semiconductor current path connected between the source and the drain regions, a plurality of small memory nodes covered by a potential barrier over the periphery of the memory nodes, a control electrode controlling a voltage of the current path and the memory nodes;

a plurality of the semiconductor memory devices storing an information by a difference of an electron charge in each memory node;

a plurality of control gates connected to each other between the plural semiconductor memory devices; and

wherein a voltage applied between the source and the drain in the semiconductor memory device is different according to the difference in information to be written in a writing operation in the plural semiconductor memory device.

--38. The semiconductor memory device according to claim 37, wherein a large voltage among the voltage applied between

the source and the drain in the semiconductor memory device is over 3 V in the writing operation of the information.

--39. The semiconductor memory device according to claim 37, wherein a small voltage among the voltage applied between the source and the drain in the semiconductor memory device is substantially 0 V in the writing operation of the information.

--40. The semiconductor memory device according to claim 37, wherein a positive/negative polarity of the voltage applied between the source and the drain in the reading operation for the stored information is opposite from a positive/negative polarity of the voltage applied between the source and the drain in the writing operation.

--41. The semiconductor memory device according to claim 37, wherein the current path is located on the insulator film.--

REMARKS

Claim 1 has been canceled without prejudice or disclaimer. New claims 37-41 have been added. Accordingly, claims 37-41 are currently pending in the application.

The specification and Abstract have been amended as in the parent application. No new matter has been added.

Examination is respectfully requested.

Respectfully submitted,

Shrinath Malur
Registration No. 34,663
Attorney for Applicants

MATTINGLY, STANGER & MALUR
1800 Diagonal Rd., Suite 370
Alexandria, Virginia 22314
(703) 684-1120
Date: November 28, 2001

MARKED UP VERSION OF REPLACED PARAGRAPHS OF THE SPECIFICATION

Page 13, second full paragraph (lines 4-8), the marked-up paragraph is as follows:

Fig. 25 [is a photograph taken by a scanning electron microscope showing] illustrates a the prototype element having memory cells of 120 bits by repeatedly using the structure of the semiconductor element of Embodiment 6 of the present invention.

Pages 35 and 36, the paragraph bridging these pages from page 35, line 24 to page 36, line 12, the marked-up paragraph is as follows:

In Fig. 24, there is shown a structure in which four present structures are repeatedly arranged to have sixteen thin film regions. In Fig. 25, moreover, there is presented an [electron-microscope photograph] illustration of a prototype element which is prepared by arranging the present structures repeatedly and by arranging memory cells of 120 bits in a matrix. In the photograph, ten control electrodes run transversely. Six sets of three low-resistance regions run longitudinally (which correspond to the low-resistance regions 1 to 3 such that two of them correspond to the thin film regions 1 and 2 for one control electrode). There are

arranged 10 x 6 x 2 = 120 thin film regions. In this large-scale memory, the writing, erasing and reading methods can be accomplished basically in an identical manner.

ABSTRACT OF THE DISCLOSURE

A semiconductor quantum memory element is disclosed which can share the terminals easily among a plurality of memory elements and can pass a high current and which is strong against noise. In order to accomplish this a control electrode is formed so as to cover the entirety of thin film regions connecting low-resistance regions. As a result, the element can have a small size and can store information with high density. Thus, a highly integrated, low power consumption non-volatile memory device can be realized with reduced size. A method of forming a memory element is also disclosed including performing the following steps of forming a first insulating layer, a second insulating layer, a first conductive layer and a layer of amorphous silicon. The amorphous silicon layer is crystallized to a polycrystalline silicon film. Semiconductor drains are deposited to form charge trapping and storage regions. A fourth insulating layer is deposited over the drains and a second conductive layer is deposited over a layer of silicon dioxide to form a control electrode of the memory element.